AMENDMENTS TO THE CLAIMS

Claim 1 (currently amended): A method for performing design verification, the method comprising:

specifying at least one hardware description language object that represents at least one signal as a symbol in a design using a first statement that is part of a hardware description language; and

instructing a symbolic simulator in response to the first statement to treat the at least one hardware description language object as a symbol.

Claim 2 (currently amended): The method defined in Claim 1 further comprising:

inserting the first statement into a design specification; and

inputting the design specification into the symbolic simulator.

Claim 3 (cancelled)

Claim 4 (currently amended): The method defined in Claim 1 wherein the at least one hardware description language object comprises a Verilog object.

Claim 5 (cancelled)

Claim 6 (original): The method defined in Claim 1 wherein the at least one signal comprises an input.

Claim 7 (currently amended): The method defined in Claim 1 further comprising:

specifying a check using a second statement that is part of the hardware description language, the check to perform a test to validate design functionality; and

instructing the symbolic simulator using the second statement to perform the test.

Claim 8 (previously presented): The method defined in Claim 7 further comprising:

inserting the first and second statements into a design specification; and

inputting the design specification into the symbolic simulator.

Claim 9 (previously presented): The method defined in Claim 7 wherein the second statement comprises a PLI.

Claim 10 (original): The method defined in Claim 7 further comprising:

instructing the symbolic simulator to generate a file with information to locate an identified fault.

Claim 11 (currently amended): An article of manufacture having at least one recordable medium having stored thereon executable instructions which, when executed by at least one processing device, cause the at least one processing device to:

specify at least one hardware description language object that represents at least one signal as a symbol in a design using a first statement that is part of a ~~design~~ hardware description language; and

instruct a symbolic simulator in response to the first statement to treat the at least one hardware description language object as a symbol.

Claim 12 (previously presented): The article of manufacture defined in Claim 11 further comprising executable instructions stored on the at least one recordable medium which, when executed by at least one processing device, cause the at least one processing device to:

insert the first statement into a design specification; and

input the design specification into the symbolic simulator.

Claim 13 (cancelled)

Claim 14 (currently amended): The article of manufacture defined in Claim 11 wherein the at least one hardware description language object comprises a Verilog object.

Claim 15 (cancelled)

Claim 16 (original): The article of manufacture defined in Claim 11 wherein the at least one signal comprises an input.

Claim 17 (currently amended): The article of manufacture defined in Claim 11 further comprising executable instructions stored on the at least one recordable medium which, when executed by at least one processing device, cause the at least one processing device to:

specify a check using a second statement that is part of the hardware description language, the check to perform a test to validate design functionality; and

instruct the symbolic simulator using the second statement to perform the test.

Claim 18 (previously presented): The article of manufacture defined in Claim 17 further comprising executable instructions stored on the at least one recordable medium which, when executed by at least one processing device, cause the at least one processing device to:

insert the first and second statements into a design specification; and

input the design specification into the symbolic simulator.

Claim 19 (previously presented): The article of manufacture defined in Claim 17 wherein the second statement comprises a PLI.

Claim 20 (original): The article of manufacture defined in Claim 17 further comprising executable instructions stored on the at least one recordable medium which, when executed by at least one processing device, cause the at least one processing device to:

instruct the symbolic simulator to generate a file with information to locate an identified fault.